IN THE CLAIMS:

<u>13.</u>	(Canceled).
<u>14.</u>	(Canceled).
<u>15.</u>	The semiconductor wafer of claim 3, wherein each chip section has a center and a
periph	ery and said interconnection layers extend from said periphery toward said center, and
wherein the plurality of chip electrodes are positioned on said periphery.	
<u>16.</u>	The semiconductor wafer of claim 4, wherein each chip section has a center and a
periph	ery and said interconnection layers extend from said periphery toward said center, and
wherei	in the plurality of chip electrodes are positioned on said periphery.
<u>17.</u>	(Canceled).
<u>18.</u>	(Canceled).
<u>19.</u>	(Canceled).
<u>20.</u>	(Canceled).
<u>21.</u>	(Canceled).
<u>22.</u>	(Canceled).
<u>23.</u>	(Canceled).
<u>24.</u>	(Canceled).
<u>25.</u>	The semiconductor wafer of claim 1, wherein said bump electrodes are arranged in a grid
array.	
<u> 26.</u>	The semiconductor wafer of claim 2, wherein said bump electrodes are arranged in a grid
arrav.	

- 27. The semiconductor wafer of claim 3, wherein said bump electrodes are arranged in a grid array.
- 28. The semiconductor wafer of claim 4, wherein said bump electrodes are arranged in a grid array.
- 29. The semiconductor wafer of claim 1, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.
- 30. The semiconductor wafer of claim 2, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.
- 31. The semiconductor wafer of claim 3, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.
- 32. The semiconductor wafer of claim 4, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.